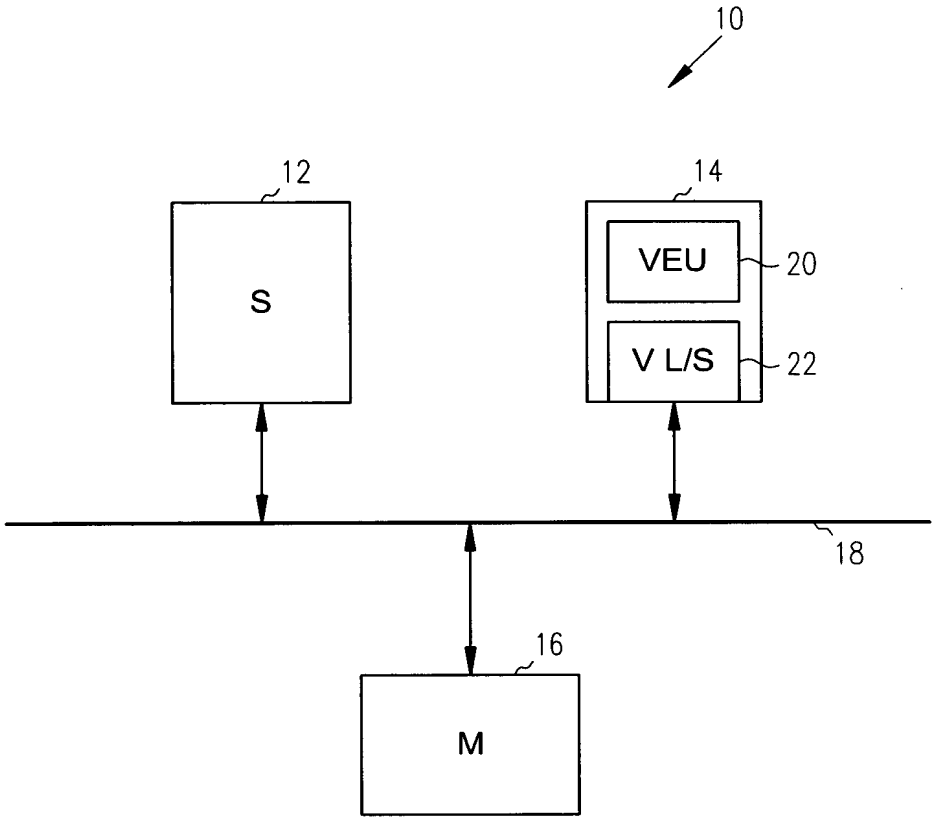

FIG. 1

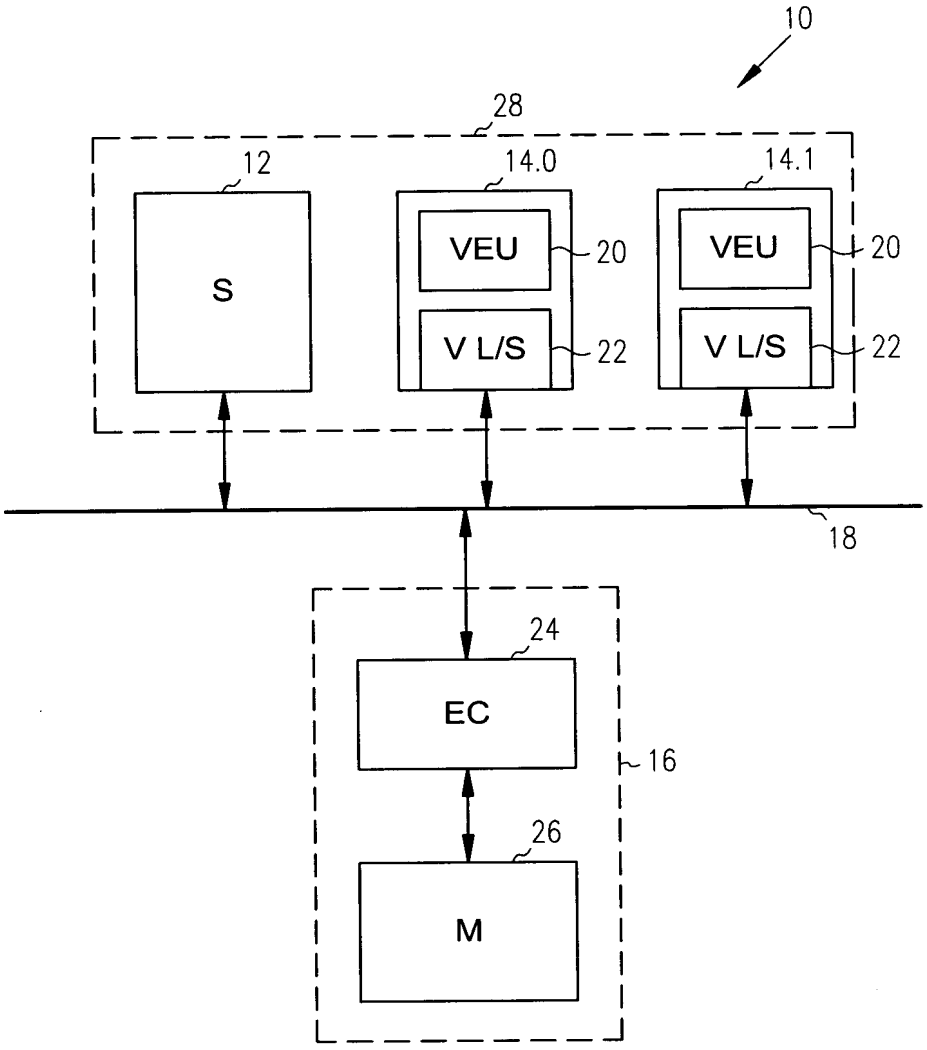

FIG. 2

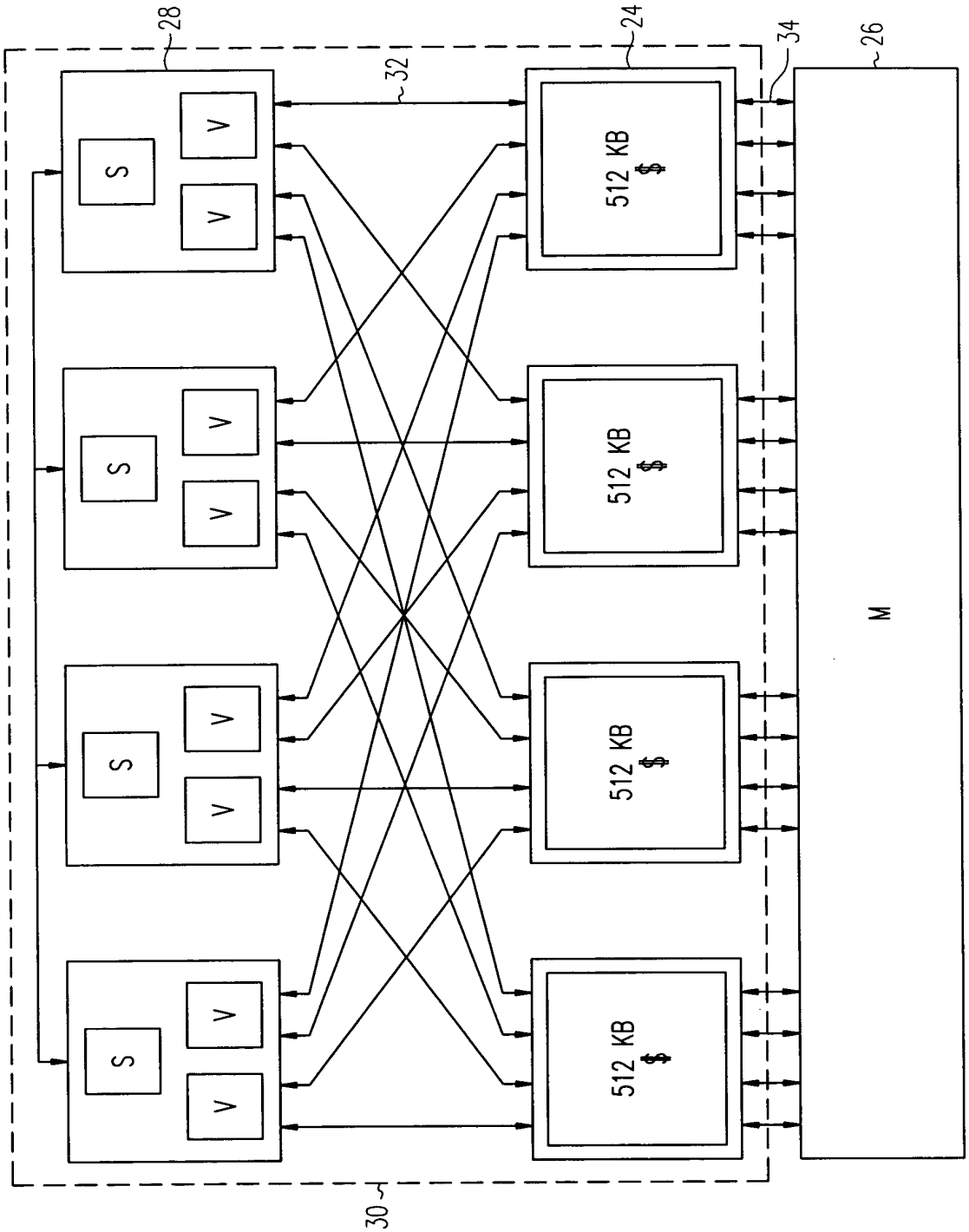

FIG. 3

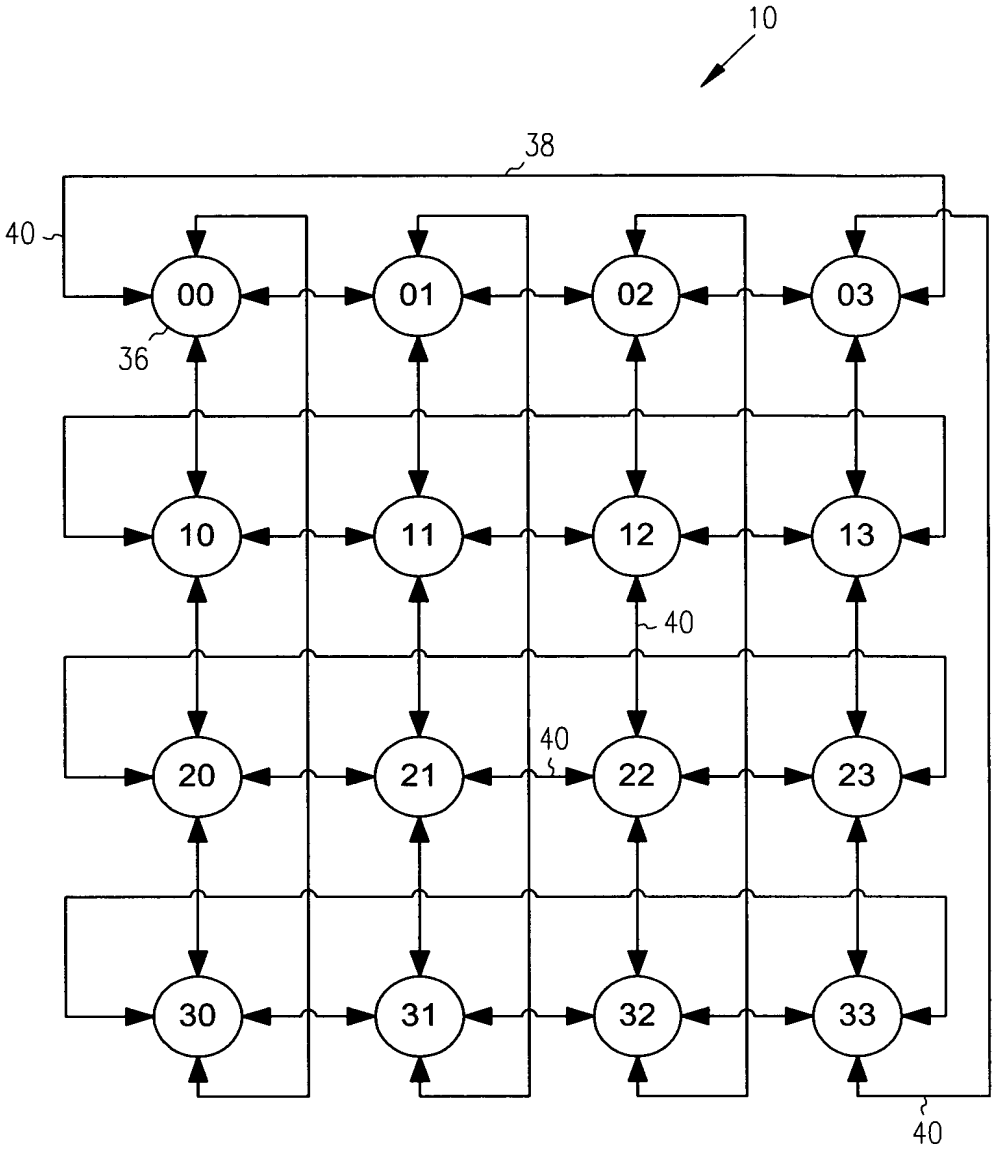

FIG. 4

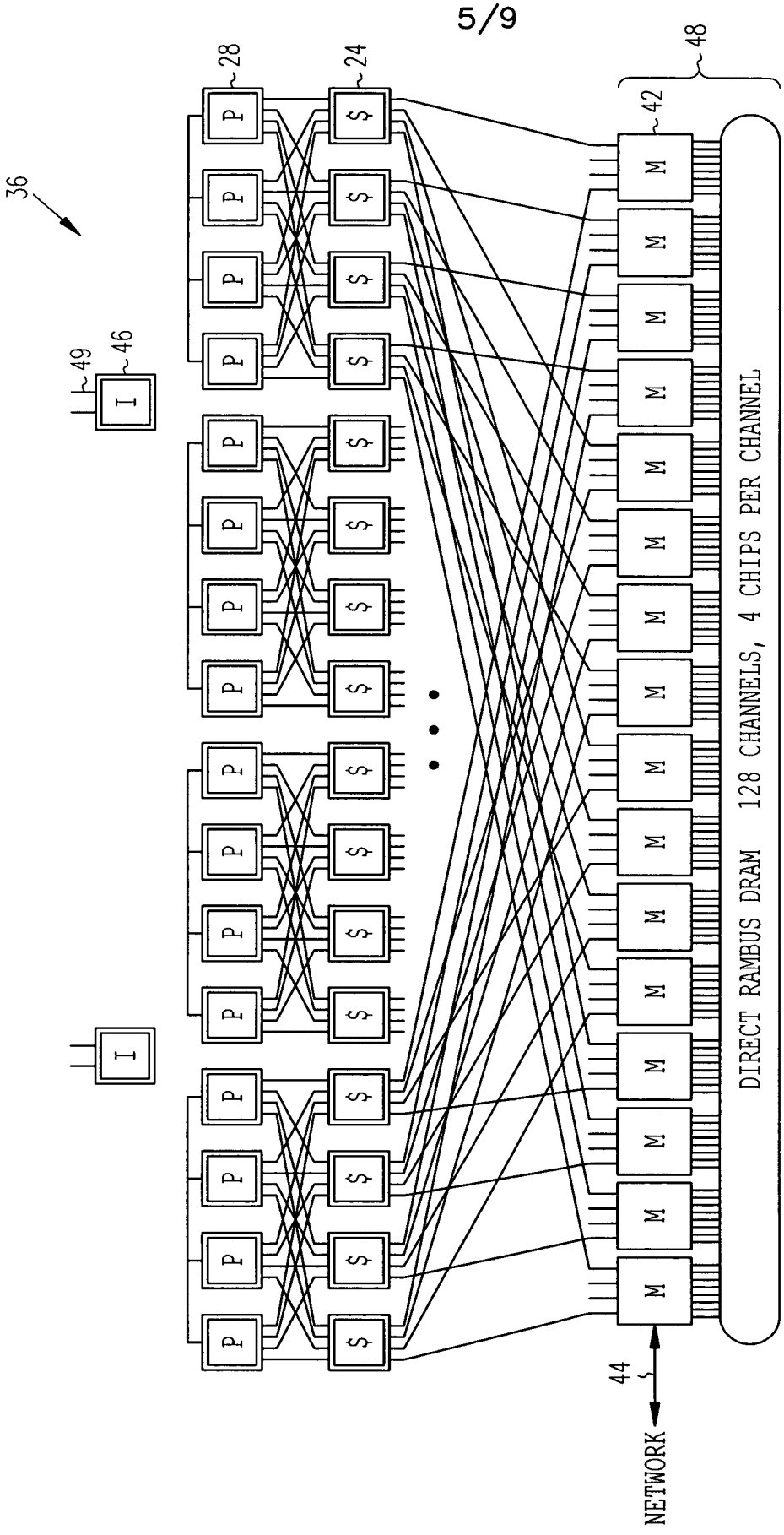
36
28
24
48
42
49
46
P
$
M
I
DIRECT RAMBUS DRAM 128 CHANNELS, 4 CHIPS PER CHANNEL
44
NETWORK

FIG. 5

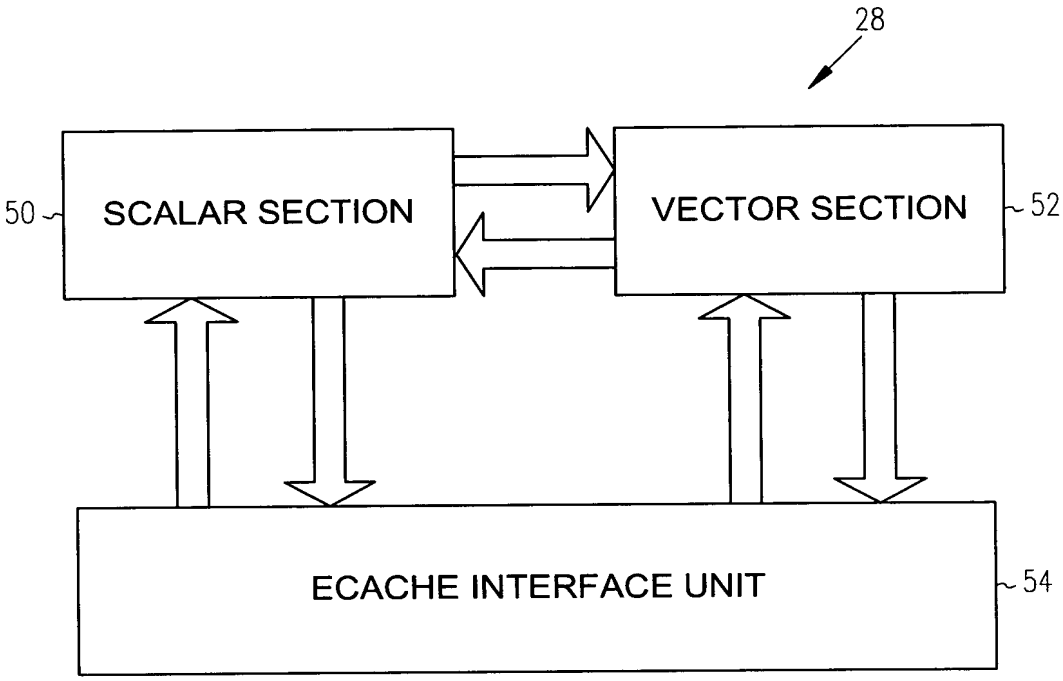
28
50
SCALAR SECTION
VECTOR SECTION
52
ECACHE INTERFACE UNIT
54

FIG. 6

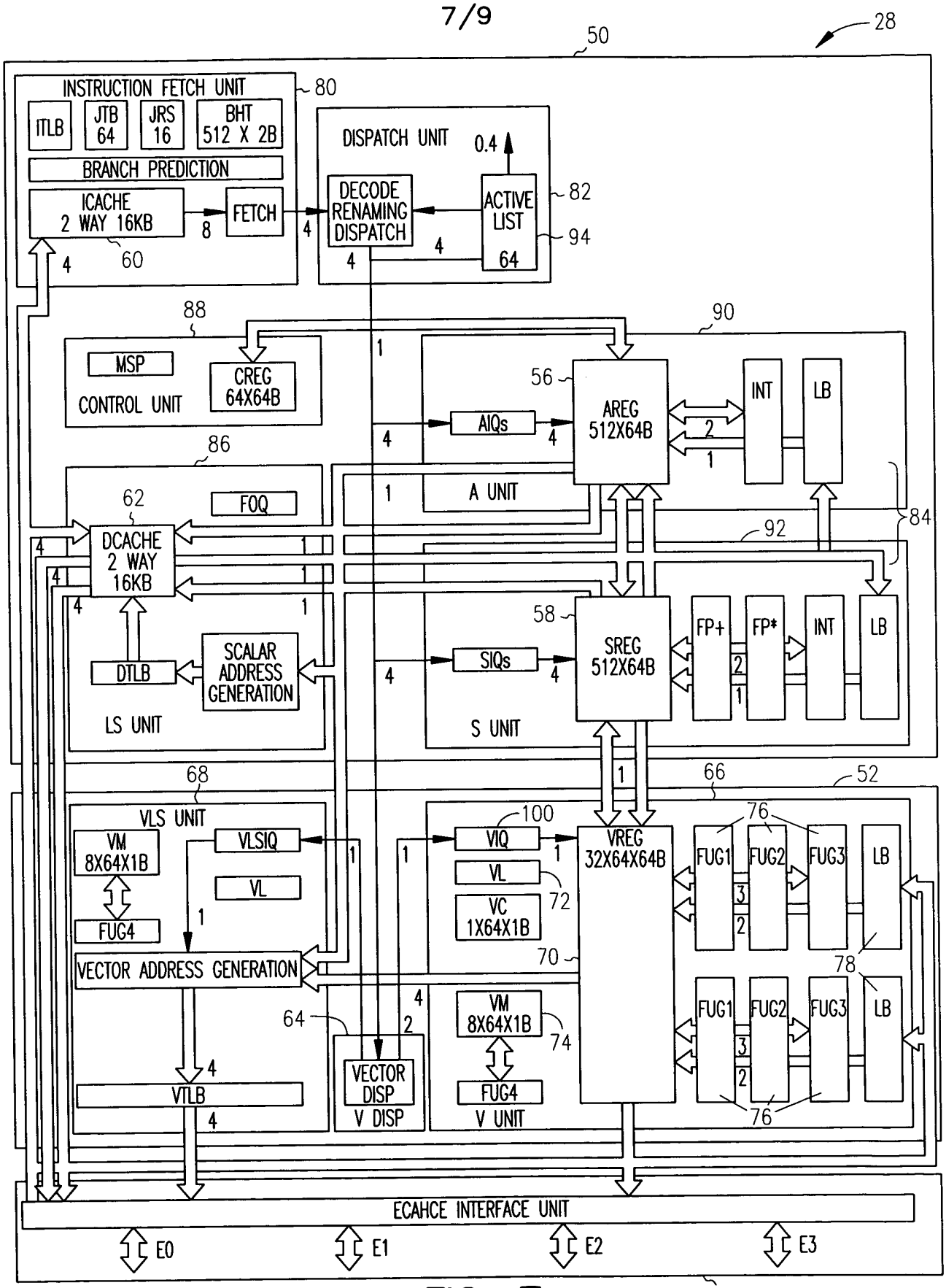
28
50
INSTRUCTION FETCH UNIT
80
ITLB
JTB 64
JRS 16
BHT 512 X 2B
BRANCH PREDICTION
ICACHE 2 WAY 16KB
FETCH
60
DISPATCH UNIT
0.4
DECODE RENAMING DISPATCH
ACTIVE LIST 64
82
94
88
90
MSP
CREG 64X64B
CONTROL UNIT
56
AIQs
AREG 512X64B
INT
LB
A UNIT
86
62
FOQ
DCACHE 2 WAY 16KB
84
92
DTLB
SCALAR ADDRESS GENERATION
LS UNIT
58
SIQs
SREG 512X64B
FP+
FP*
INT
LB
S UNIT
68
66
52
VLS UNIT
VM 8X64X1B
VLSIQ
VL
FUG4
VECTOR ADDRESS GENERATION
100
VIQ
VL
VC 1X64X1B
72
70
VREG 32X64X64B
FUG1
FUG2
FUG3
LB
76
78
64
VM 8X64X1B
74
VTLB
VECTOR DISP
V DISP
FUG4
V UNIT
ECAHCE INTERFACE UNIT
E0
E1
E2
E3
54

FIG. 7

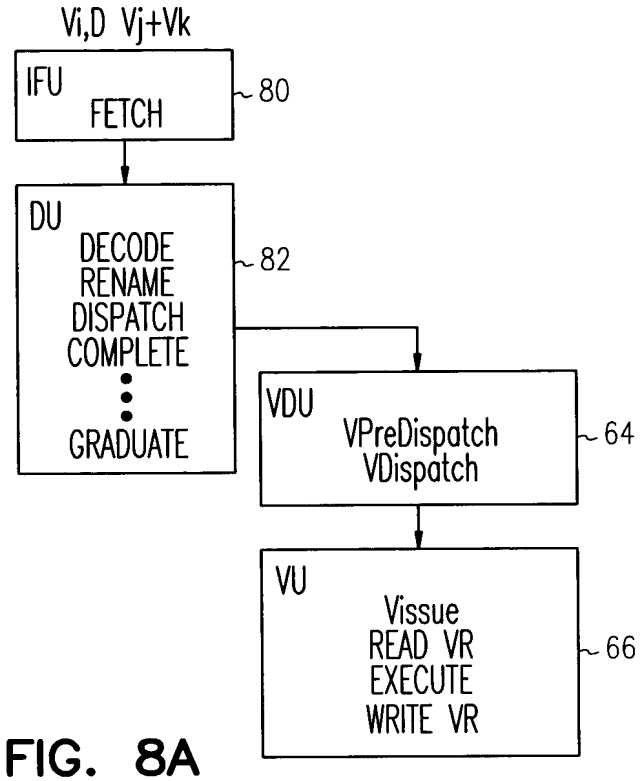
Vi,D Vj+Vk
IFU
FETCH
80
DU
DECODE
RENAME
DISPATCH
COMPLETE
GRADUATE
82
VDU
VPreDispatch
VDispatch
64
VU
Vissue
READ VR
EXECUTE
WRITE VR
66

FIG. 8A

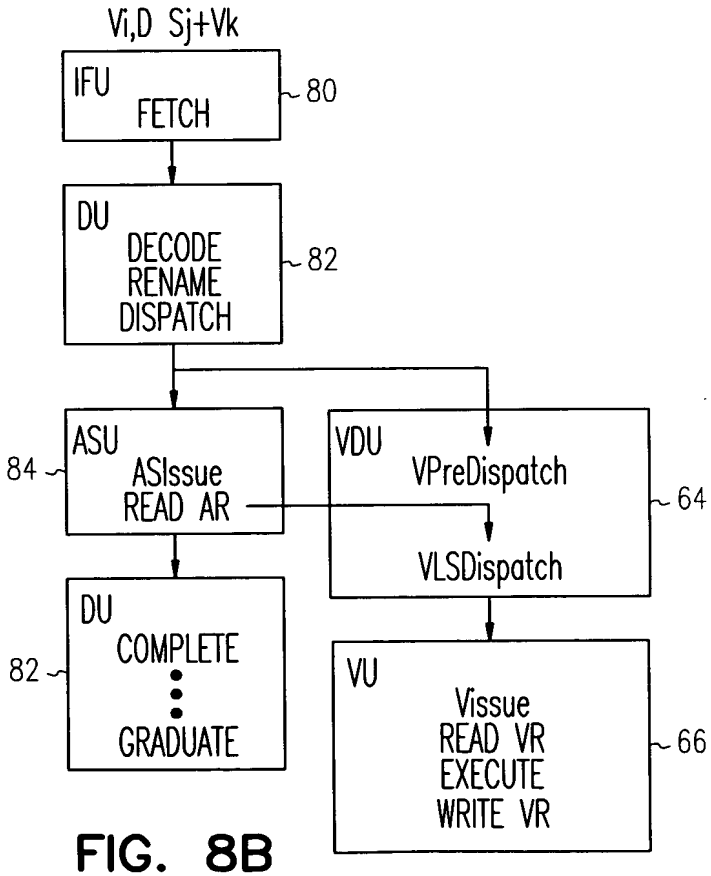
Vi,D Sj+Vk
IFU
FETCH
80
DU
DECODE
RENAME
DISPATCH
82
ASU
ASIssue
READ AR
84
VDU
VPreDispatch
VLSDispatch
64
DU
COMPLETE
GRADUATE
82
VU
Vissue
READ VR
EXECUTE
WRITE VR
66

FIG. 8B

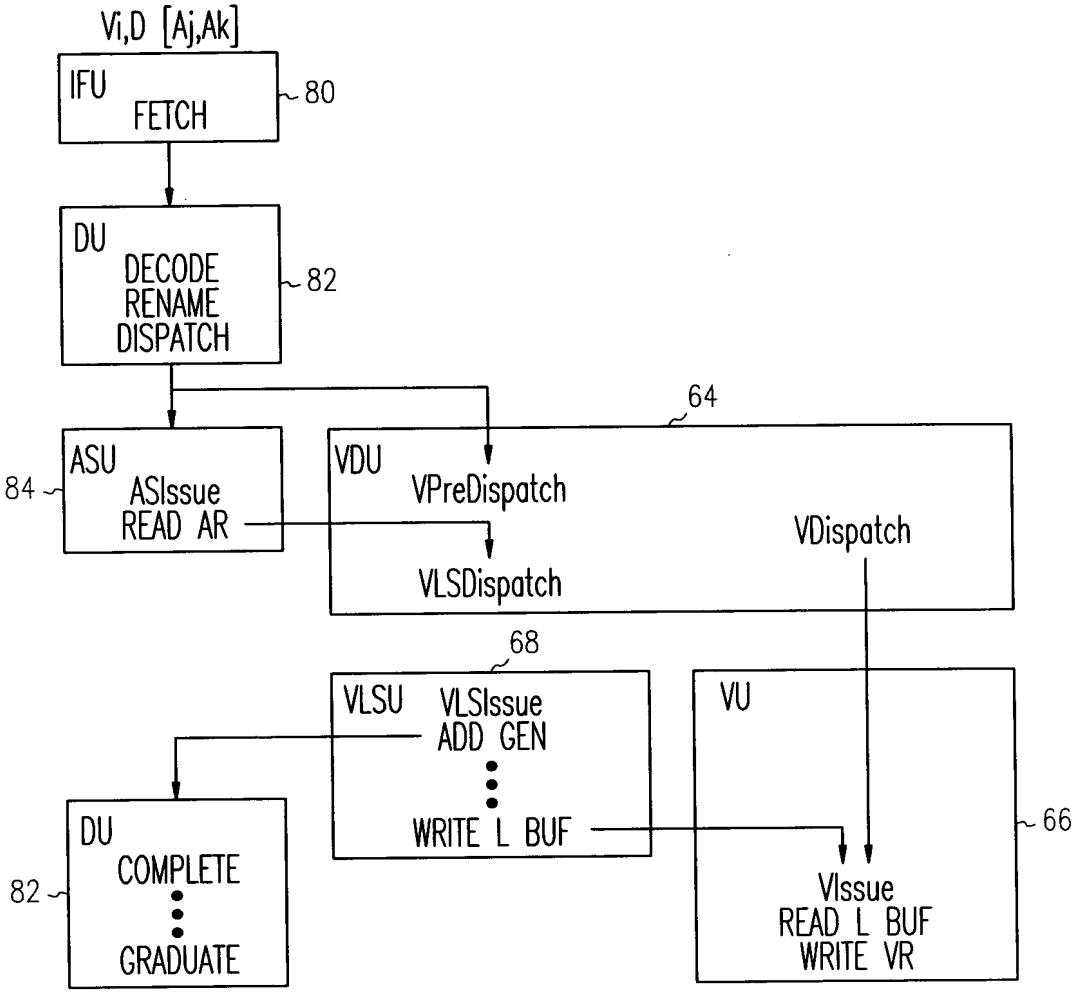
Vi,D [Aj,Ak]
IFU
FETCH
80
DU
DECODE
RENAME
DISPATCH
82
64
ASU
ASIssue
READ AR
84
VDU
VPreDispatch
VLSDispatch
VDispatch
68
VLSU
VLSIssue
ADD GEN
WRITE L BUF
VU
66
DU
COMPLETE
GRADUATE
82
VIssue
READ L BUF
WRITE VR

FIG. 8C